ABSRACT OF THE DISCLOSURE

A semiconductor memory device includes an SRAM provided on a chip, the SRAM including an SRAM cell array. A DRAM is provided on the chip, the DRAM including a DRAM cell array. An address input circuit receives an address signal, the address signal having a first portion and a second portion, the first portion carrying a unique value of row-column address information provided to access one of memory locations in one of the SRAM and DRAM cell arrays, the second portion carrying a unique value of SRAM/DRAM address information provided to select one of the SRAM and the DRAM.